

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An integrated circuit ~~comprises~~ comprising one or more integrated circuit elements and one or more input/output pins, the one or more integrated circuit elements including an interface element for interfacing with external test circuitry, the interface element communicating with the external test circuitry via a single input/output pin dedicated for testing wherein the single pin ~~connected~~ operates with several logic thresholds and wherein if an input signal on the input/output pin is in a first range defined by the logic thresholds for a first predetermined finite period of time after a power on reset, the integrated circuit is placed in a test mode, and when the integrated circuit is in the test mode, if the input signal on the input/output pin is in a second range defined by the logic thresholds ~~the external test circuitry is free from maintaining the integrated circuit in a test mode for a second~~ predetermined finite period of time, the integrated circuit defaults from the test mode to a normal mode, otherwise when the integrated circuit is in the test mode and the input signal on the input/output pin is not in the second range for the second predetermined finite period of time, the integrated circuit continues to operate in the test mode.

2. (Currently amended) An integrated circuit according to Claim 1 wherein the interface element is embedded into the integrated circuit as a single pin interface between the ~~digital~~ integrated circuit and the external test circuitry.

3. (Currently amended) An integrated circuit according to Claim 2 wherein the interface element receives test data and commands from the external test circuitry in response to which a crash block controls and commands scan path elements within the ~~digital~~ integrated circuit and returns ~~the~~ resulting data to the external test circuitry.

4. (Previously presented) An integrated circuit according to Claim 1 wherein the logic thresholds define several logic levels which enable data and timing signals to be differentiated on a single pin.

5. (Currently amended) An integrated circuit according to Claim 1 wherein a “pad detection” detector determines whether there is a connection with an external tester or other external circuitry by assessing ~~the~~a voltage on the single pin.

6. (Previously presented) An integrated circuit according to Claim 1 wherein if a voltage on the single pin is held at a voltage below “low” for a period of time determined by an “escape 0 timer” then the integrated circuit will decide there is no tester connected to the single pin.